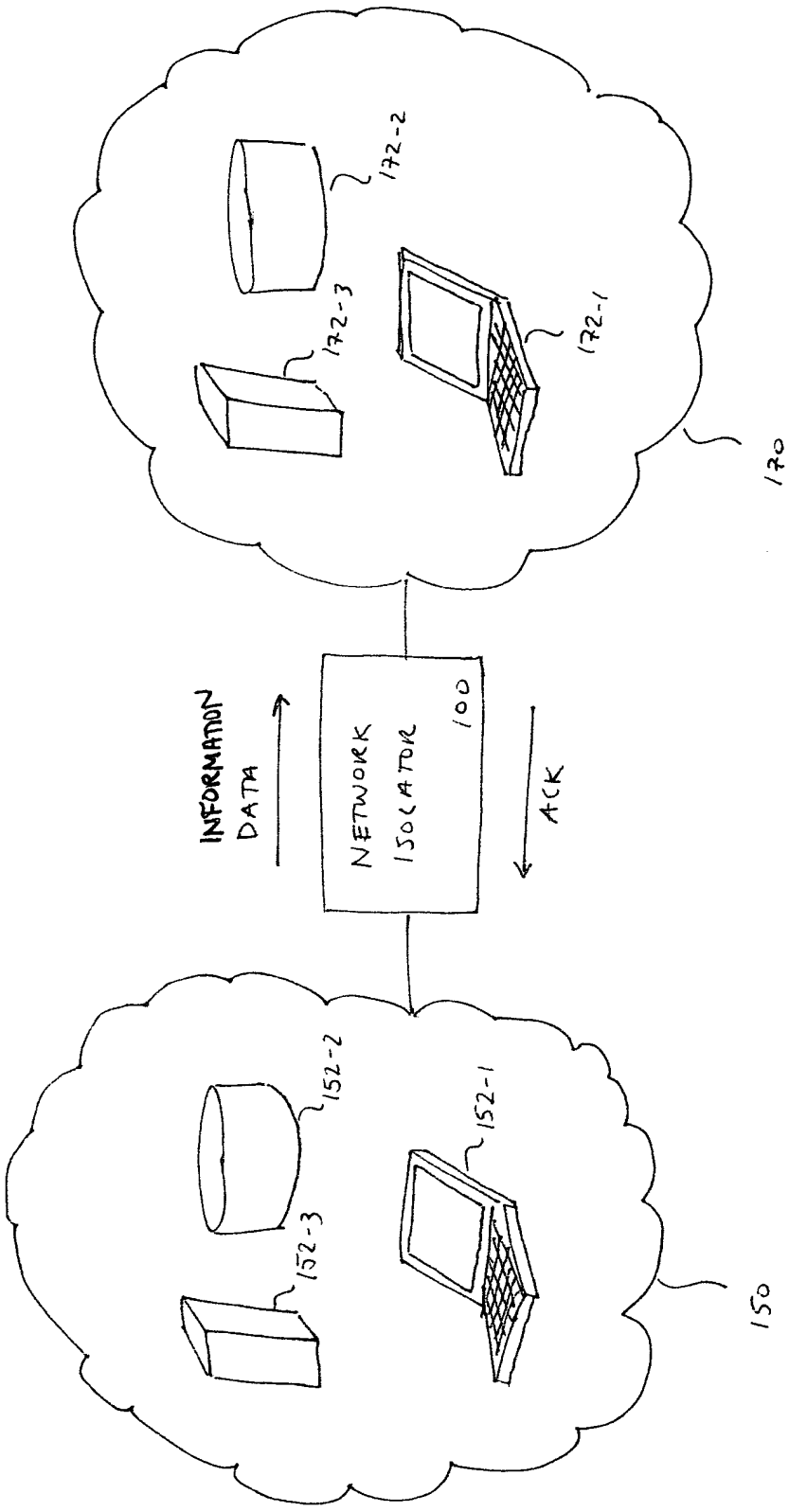
172-2
172-3
172-1
120
INFORMATION
DATA
NETWORK
ISOLATOR
100
ACK
152-2
152-1
152-3
150

Fig. 1A

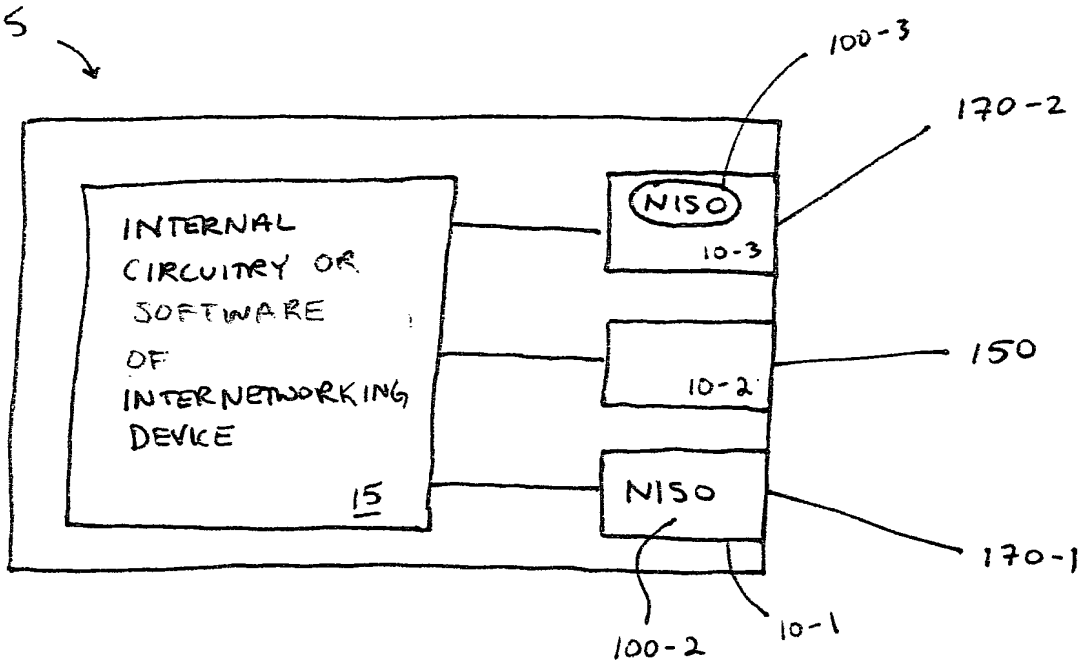
5
100-3
170-2
INTERNAL CIRCUITRY OR SOFTWARE OF INTERNETWORKING DEVICE
15
NISO
10-3
10-2
150
NISO
170-1
100-2
10-1

FIG. 1B

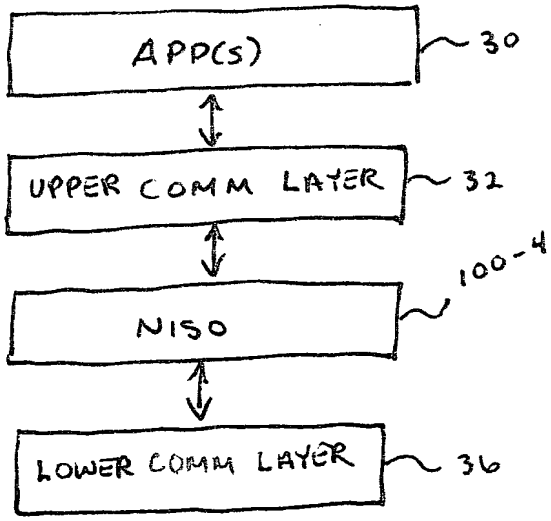
APP(S)
30
UPPER COMM LAYER
32
NISO
100-4
LOWER COMM LAYER
36

FIG. 1C

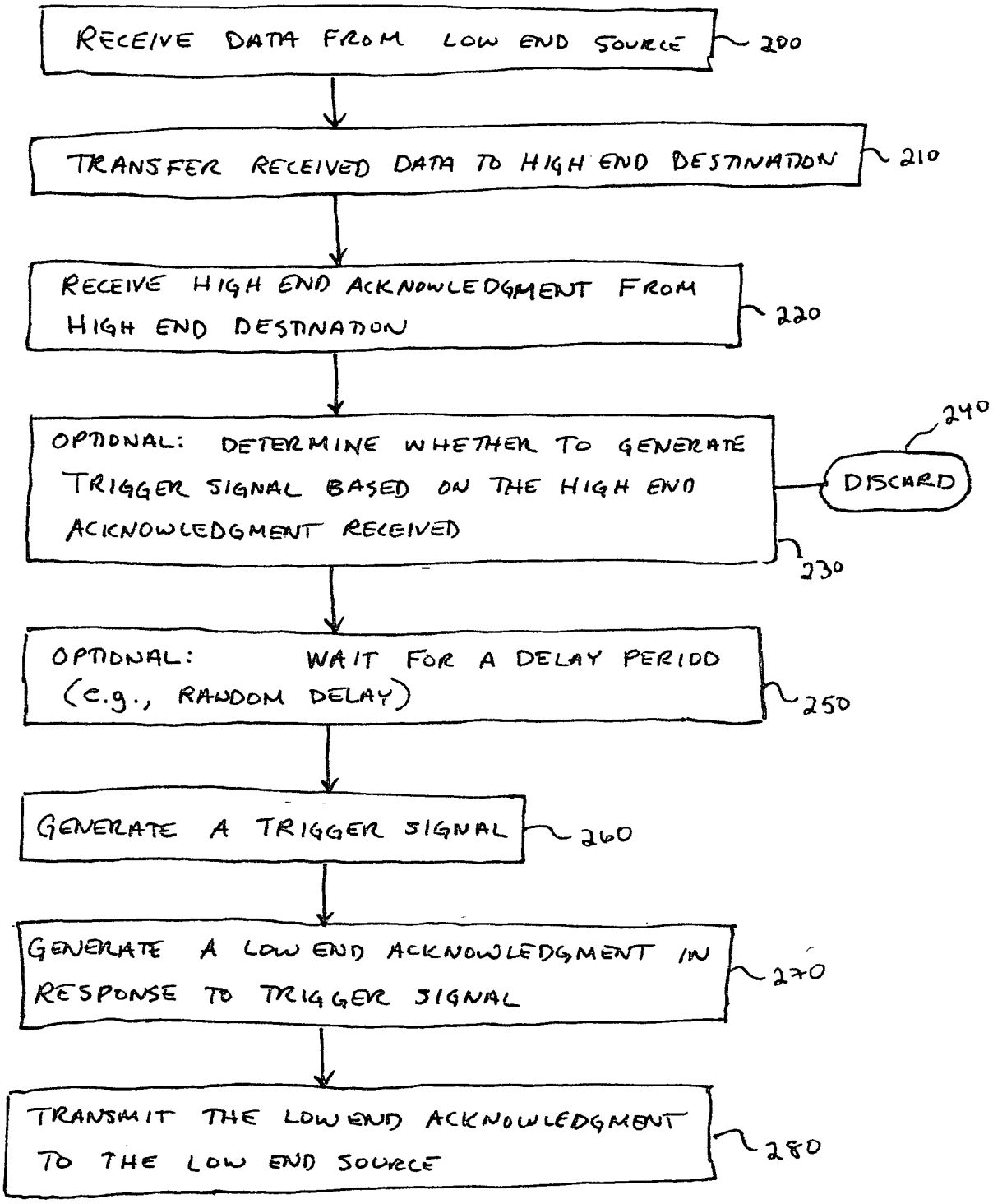
RECEIVE DATA FROM LOW END SOURCE
200
TRANSFER RECEIVED DATA TO HIGH END DESTINATION
210
RECEIVE HIGH END ACKNOWLEDGMENT FROM HIGH END DESTINATION
220
OPTIONAL: DETERMINE WHETHER TO GENERATE TRIGGER SIGNAL BASED ON THE HIGH END ACKNOWLEDGMENT RECEIVED
230
240
DISCARD
OPTIONAL: WAIT FOR A DELAY PERIOD (e.g., RANDOM DELAY)
250
GENERATE A TRIGGER SIGNAL
260
GENERATE A LOW END ACKNOWLEDGMENT IN RESPONSE TO TRIGGER SIGNAL
270
TRANSMIT THE LOW END ACKNOWLEDGMENT TO THE LOW END SOURCE
280

FIG. 2

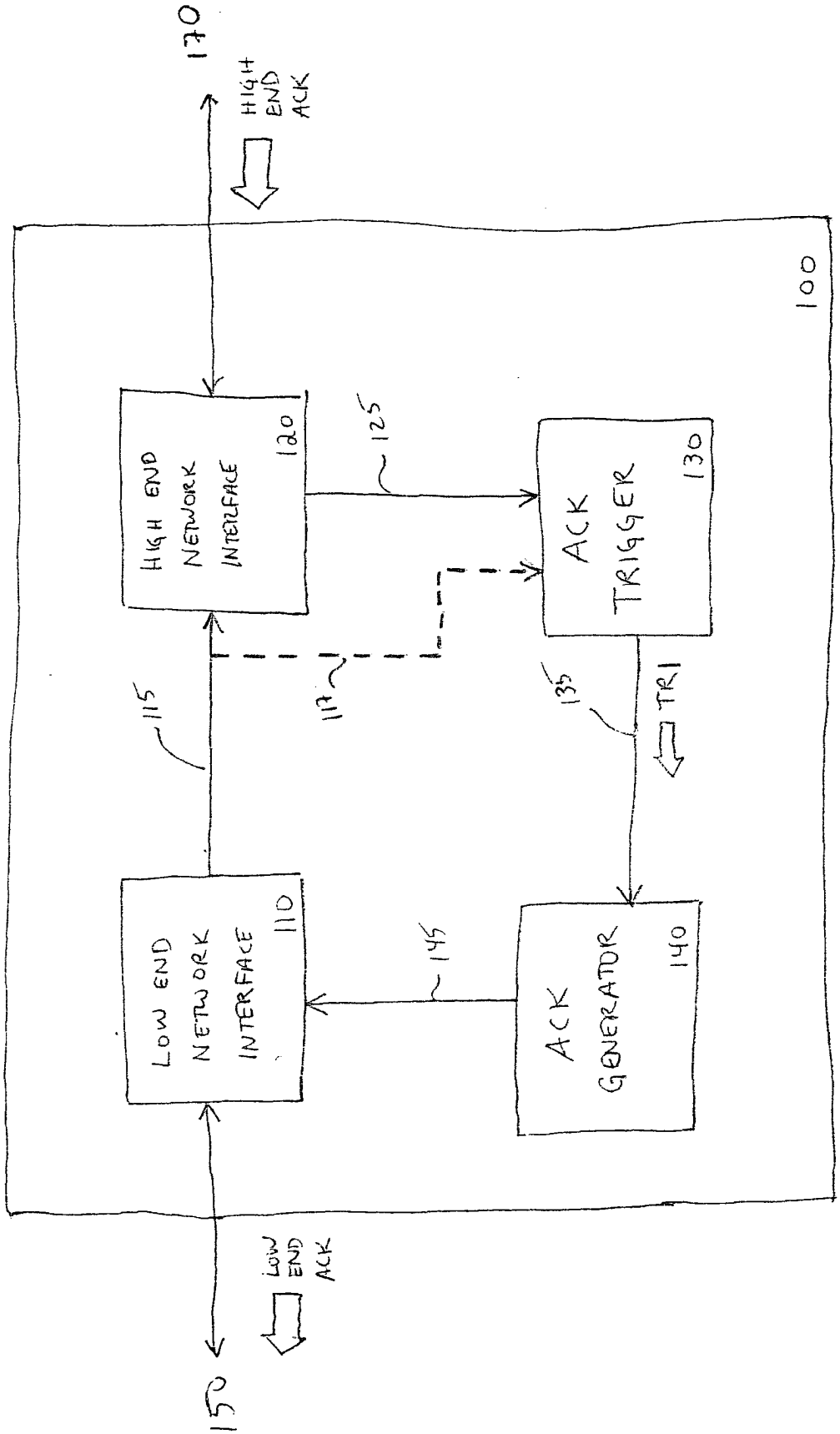
170
HIGH END ACK
100
HIGH END NETWORK INTERFACE
120
125
ACK TRIGGER
130
115
117
135
TRI
LOW END NETWORK INTERFACE
110
145
ACK GENERATOR
140
LOW END ACK
150

Fig. 3

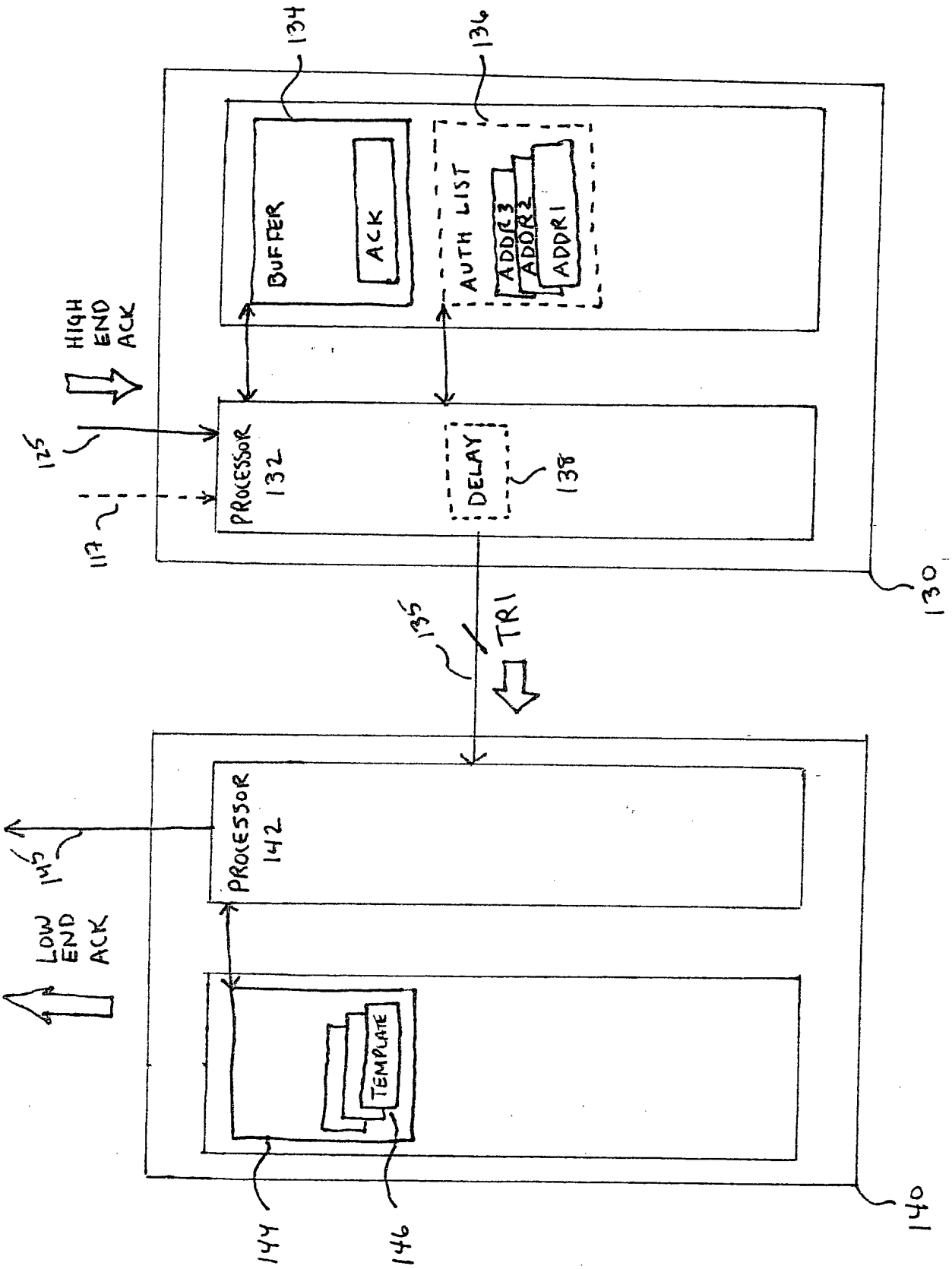
134
136
BUFFER
ACK
AUTH LIST
ADDR3
ADDR2
ADDR1
HIGH END ACK
125
PROCESSOR 132
117
DELAY
138
130
135
TRI
PROCESSOR 142
145
LOW END ACK
TEMPLATE
144
146
140

FIG. 4

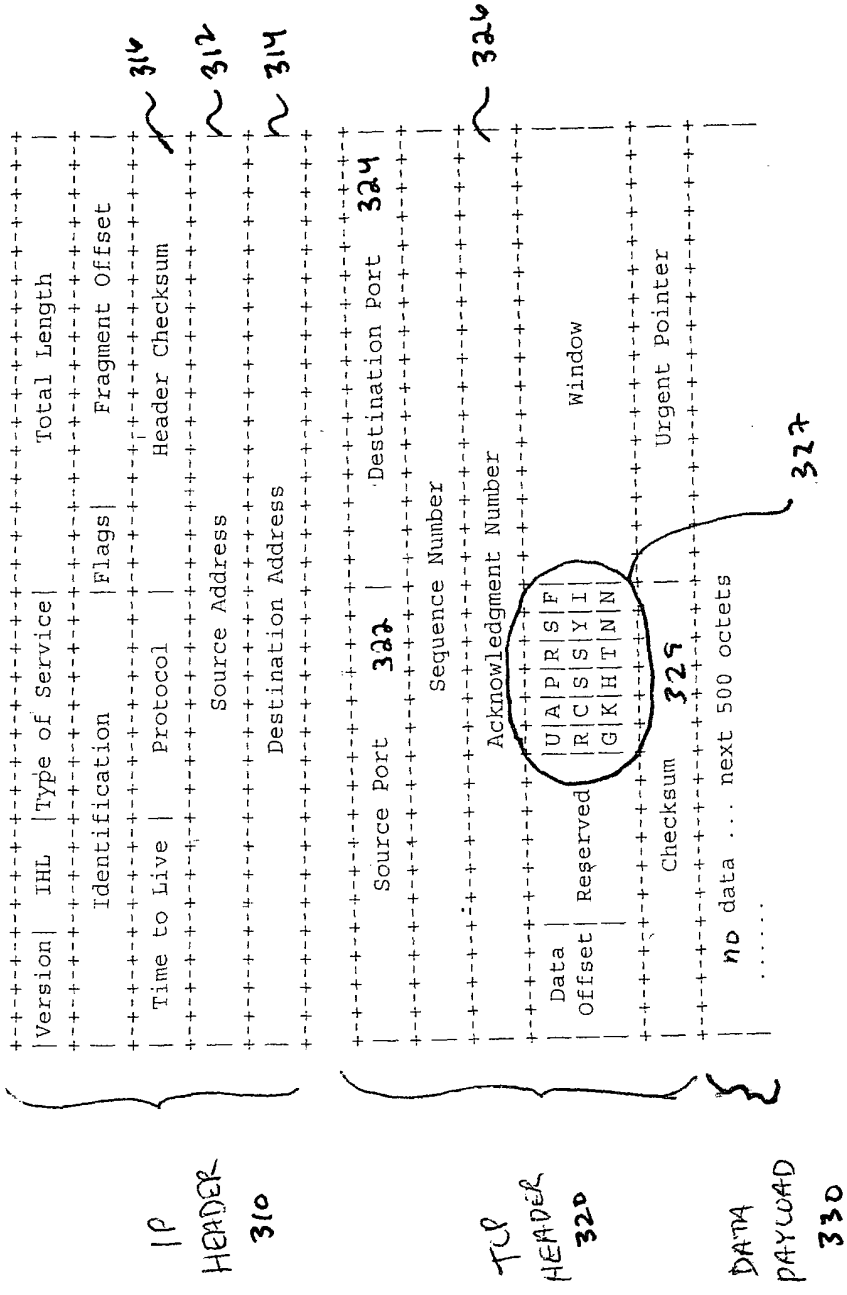
Version
IHL
Type of Service
Total Length
Identification
Flags
Fragment Offset
Time to Live
Protocol
Header Checksum
Source Address
Destination Address
IP HEADER 310
Source Port
Destination Port
Sequence Number
Acknowledgment Number
Data Offset
Reserved
URG
ACK
PSH
RST
SYN
FIN
Window
Checksum
Urgent Pointer
no data ... next 500 octets
TCP HEADER 320
DATA PAYLOAD 330
312
314
316
322
324
326
327
328

Fig. 5

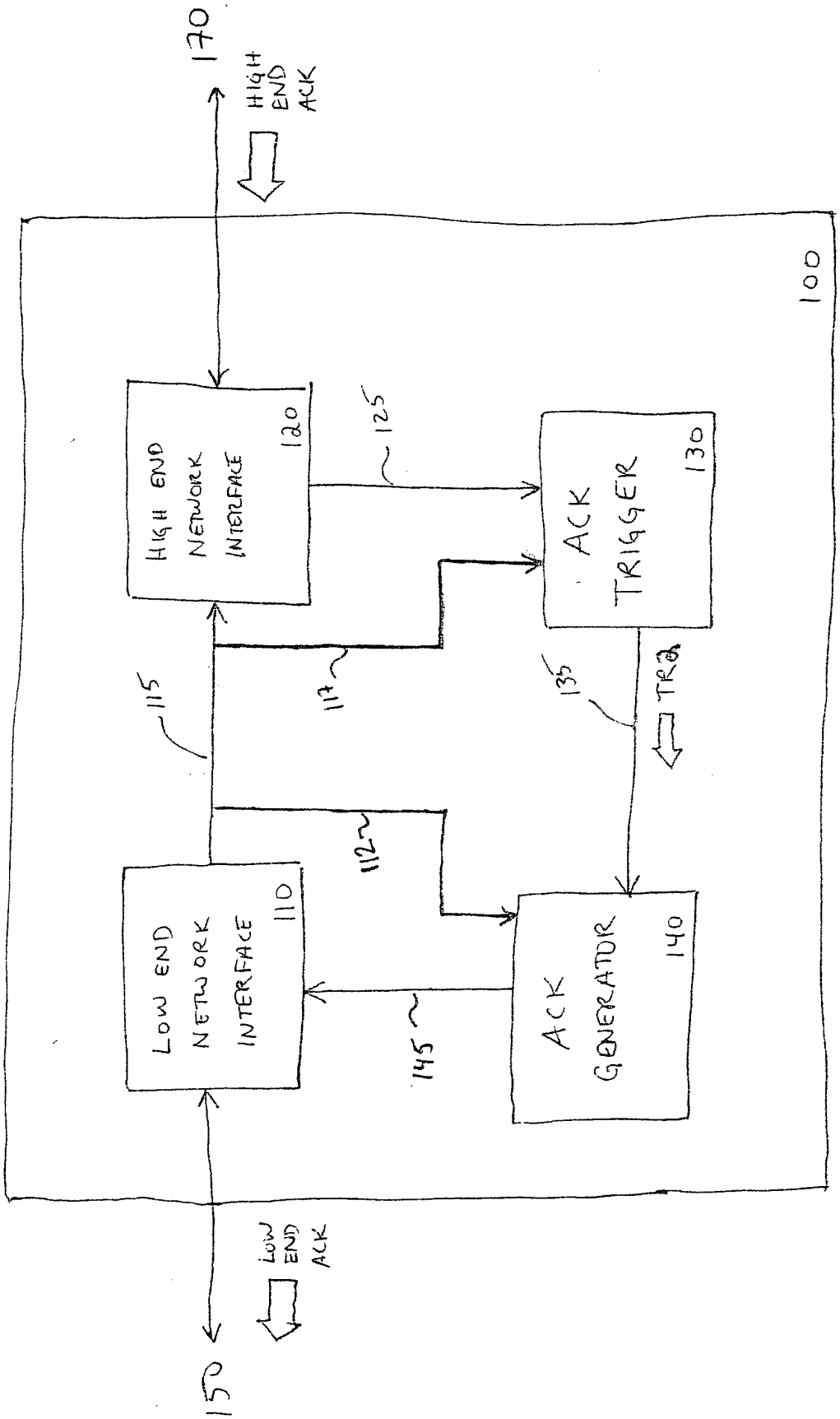
170
HIGH END ACK
100
HIGH END NETWORK INTERFACE
120
125
ACK TRIGGER
130
117
135
TRG
115
112
LOW END NETWORK INTERFACE
110
ACK GENERATOR
140
145
LOW END ACK
150

Fig. 6

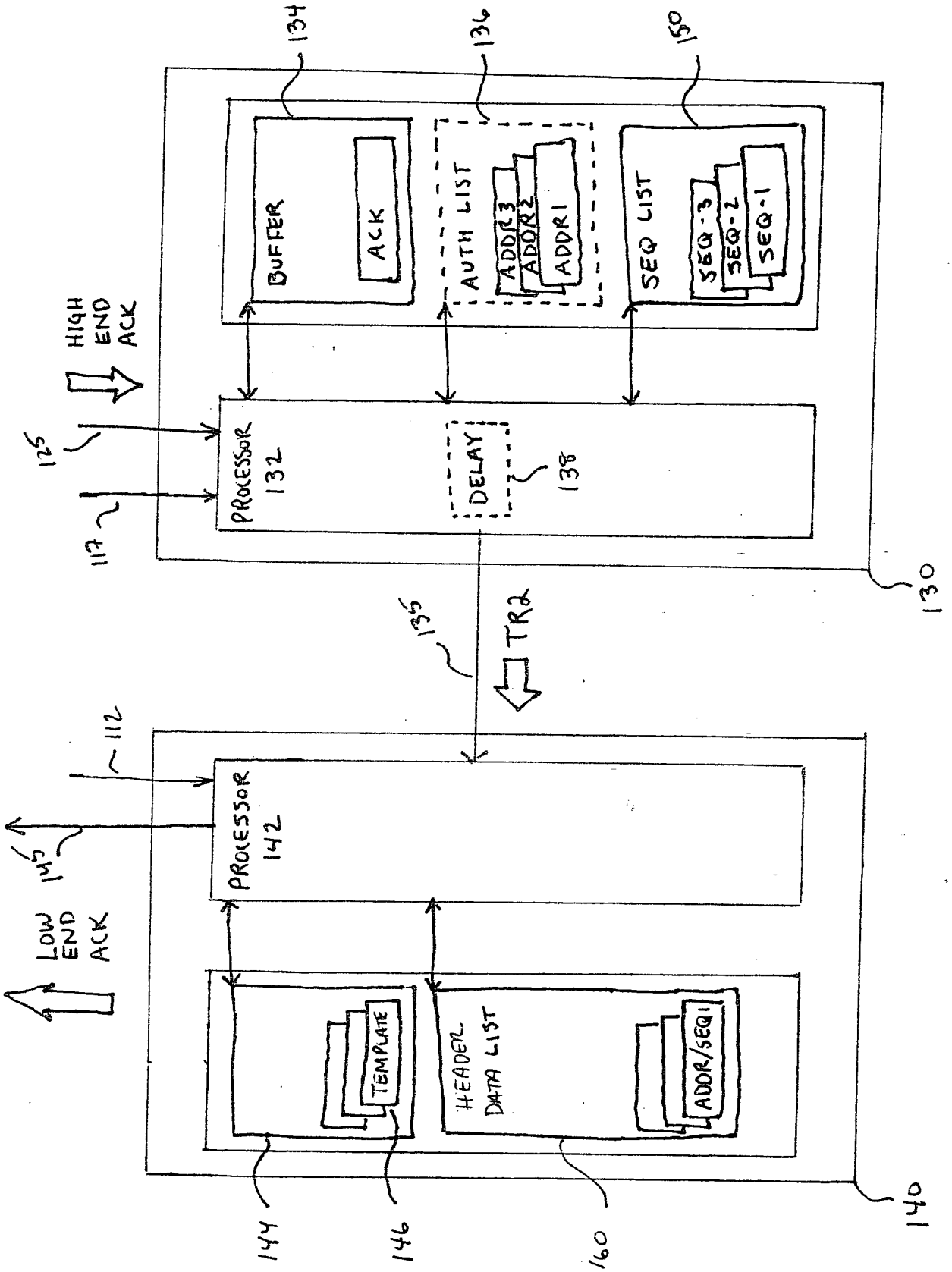
134
136
150
BUFFER
ACK
AUTH LIST
ADDR3
ADDR2
ADDR1
SEQ LIST
SEQ-3
SEQ-2
SEQ-1
HIGH END ACK
125
117
PROCESSOR 132
DELAY
138
130
135
TR2
112
PROCESSOR 142
145
LOW END ACK
TEMPLATE
HEADER DATA LIST
ADDR/SEQ1
144
146
160
140

Fig. 7

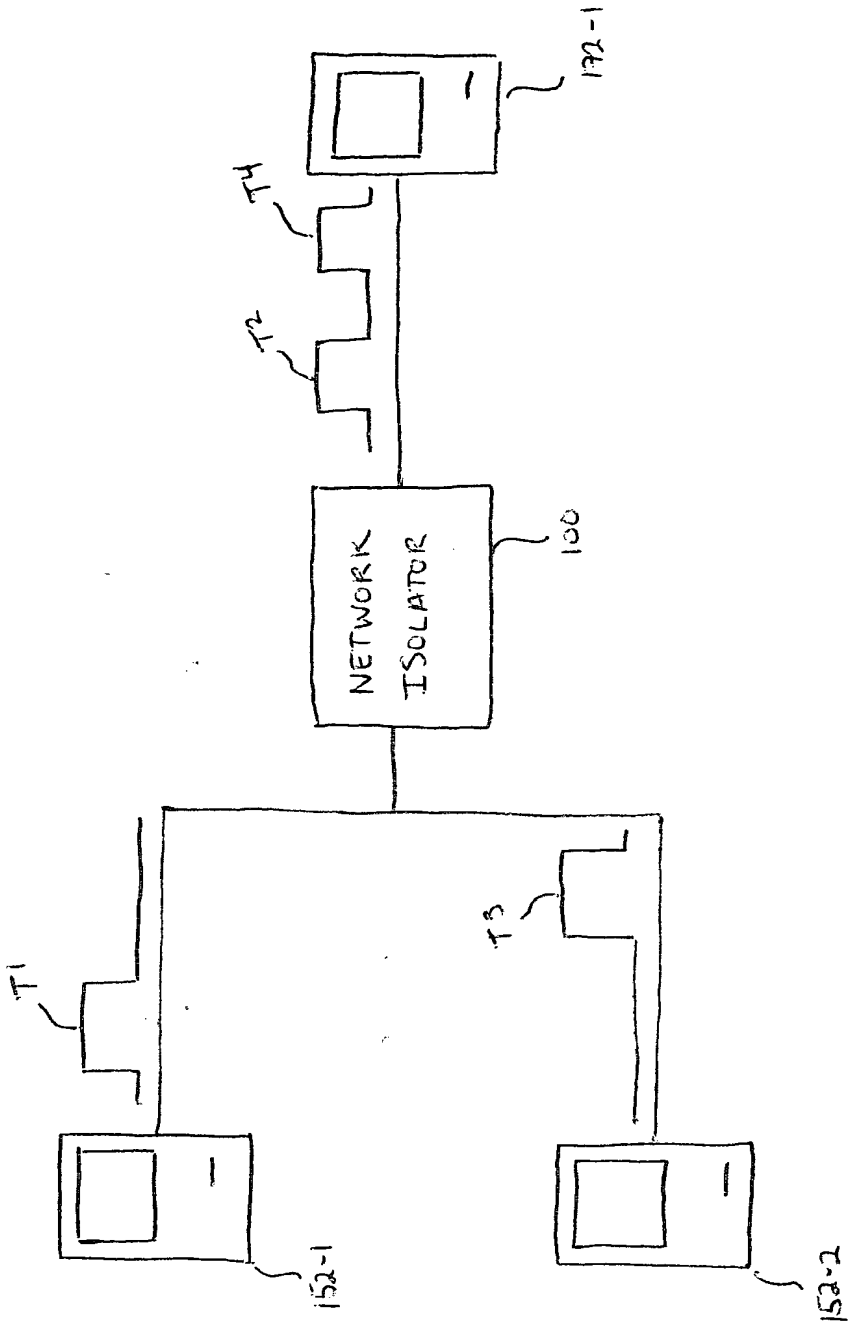

FIG. 8

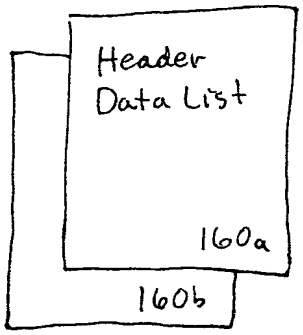

Fig. 9A

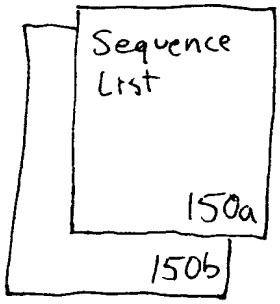

Fig. 9B

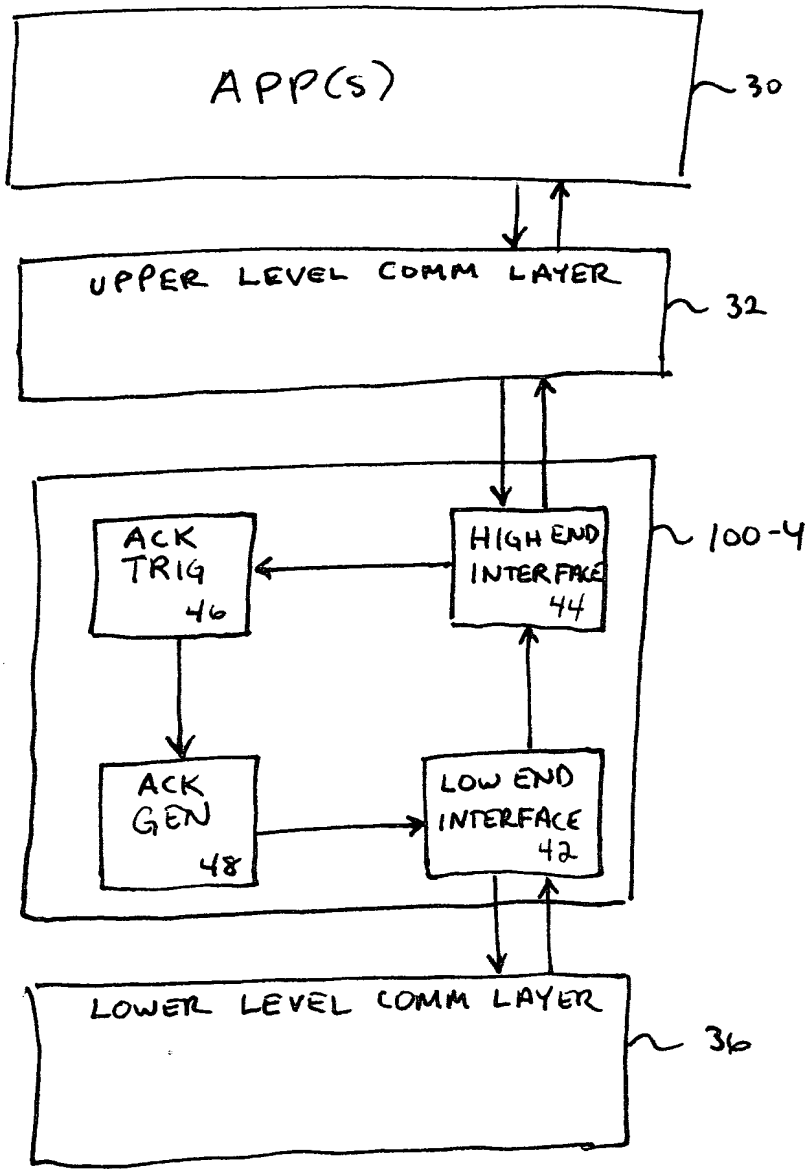
APP(S)
30
UPPER LEVEL COMM LAYER
32
ACK TRIG 46
HIGH END INTERFACE 44
100-4
ACK GEN 48
LOW END INTERFACE 42
LOWER LEVEL COMM LAYER
36

Fig. 10